• Microprocessor Peripheral or Standalone Operation
• 8-Bit Resolution A/D Converter
• Differential Reference Input Voltages
• Conversion Time \( \ldots 17 \, \mu s \) Max
• Total Access and Conversion Cycles Per Second
  – TLC548 \ldots \) up to 45 500
  – TLC549 \ldots \) up to 40 000
• On-Chip Software-Controllable Sample-and-Hold Function
• Total Unadjusted Error \( \ldots \pm 0.5 \) LSB Max
• 4-MHz Typical Internal System Clock
• Wide Supply Range \( \ldots 3 \, V \) to 6 \, V
• Low Power Consumption \( \ldots 15 \, mW \) Max
• Ideal for Cost-Effective, High-Performance Applications including Battery-Operated Portable Instrumentation
• Pinout and Control Signals Compatible With the TLC540 and TLC545 8-Bit A/D Converters and with the TLC1540 10-Bit A/D Converter
• CMOS Technology

description

The TLC548 and TLC549 are CMOS analog-to-digital converter (ADC) integrated circuits built around an 8-bit switched-capacitor successive-approximation ADC. These devices are designed for serial interface with a microprocessor or peripheral through a 3-state data output and an analog input. The TLC548 and TLC549 use only the input/output clock (I/O CLOCK) input along with the chip select (CS) input for data control. The maximum I/O CLOCK input frequency of the TLC548 is 2.048 MHz, and the I/O CLOCK input frequency of the TLC549 is specified up to 1.1 MHz.

AVAILABLE OPTIONS

<table>
<thead>
<tr>
<th>TA</th>
<th>PACKAGE</th>
<th>TYPICAL VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMALL OUTLINE (D)</td>
<td>PLASTIC DIP (P)</td>
<td></td>
</tr>
<tr>
<td>0°C to 70°C</td>
<td>TLC548CD</td>
<td>TLC548CP</td>
</tr>
<tr>
<td>8°C to 75°C</td>
<td>TLC549CD</td>
<td>TLC549CP</td>
</tr>
</tbody>
</table>

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
Operation of the TLC548 and the TLC549 is very similar to that of the more complex TLC540 and TLC541 devices; however, the TLC548 and TLC549 provide an on-chip system clock that operates typically at 4 MHz and requires no external components. The on-chip system clock allows internal device operation to proceed independently of serial input/output data timing and permits manipulation of the TLC548 and TLC549 as desired for a wide range of software and hardware requirements. The I/O CLOCK together with the internal system clock allow high-speed data transfer and conversion rates of 45 500 conversions per second for the TLC548, and 40 000 conversions per second for the TLC549.

Additional TLC548 and TLC549 features include versatile control logic, an on-chip sample-and-hold circuit that can operate automatically or under microprocessor control, and a high-speed converter with differential high-impedance reference voltage inputs that ease ratiometric conversion, scaling, and circuit isolation from logic and supply noises. Design of the totally switched-capacitor successive-approximation converter circuit allows conversion with a maximum total error of ±0.5 least significant bit (LSB) in less than 17 µs.

The TLC548C and TLC549C are characterized for operation from 0°C to 70°C. The TLC548I and TLC549I are characterized for operation from –40°C to 85°C.
operating sequence

NOTES:  
A. The conversion cycle, which requires 36 internal system clock periods (17 µs maximum), is initiated with the eighth I/O clock pulse trailing edge after CS goes low for the channel whose address exists in memory at the time.

B. The most significant bit (A7) is automatically placed on the DATA OUT bus after CS is brought low. The remaining seven bits (A6–A0) are clocked out on the first seven I/O clock falling edges. B7–B0 follows in the same manner.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Specification</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, $V_{CC}$ (see Note 1)</td>
<td>$6.5 \text{ V}$</td>
</tr>
<tr>
<td>Input voltage range at any input</td>
<td>$-0.3 \text{ V to } V_{CC} + 0.3 \text{ V}$</td>
</tr>
<tr>
<td>Output voltage range</td>
<td>$-0.3 \text{ V to } V_{CC} + 0.3 \text{ V}$</td>
</tr>
<tr>
<td>Peak input current range (any input)</td>
<td>$\pm 10 \text{ mA}$</td>
</tr>
<tr>
<td>Peak total input current range (all inputs)</td>
<td>$\pm 30 \text{ mA}$</td>
</tr>
<tr>
<td>Operating free-air temperature range, $T_A$ (see Note 2): TLC548C, TLC549C</td>
<td>$0^\circ \text{C to } 70^\circ \text{C}$</td>
</tr>
<tr>
<td>TLC548I, TLC549I</td>
<td>$-40^\circ \text{C to } 85^\circ \text{C}$</td>
</tr>
<tr>
<td>Storage temperature range, $T_{stg}$</td>
<td>$-65^\circ \text{C to } 150^\circ \text{C}$</td>
</tr>
<tr>
<td>Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds</td>
<td>$260^\circ \text{C}$</td>
</tr>
</tbody>
</table>

NOTES:  
1. All voltage values are with respect to the network ground terminal with the REF– and GND terminals connected together, unless otherwise noted.

2. The D package is not recommended below $-40^\circ \text{C}$. 
TLC548C, TLC548I, TLC549C, TLC549I
8-BIT ANALOG-TO-DIGITAL CONVERTERS
WITH SERIAL CONTROL

**Recommended Operating Conditions**

<table>
<thead>
<tr>
<th>Condition</th>
<th>TLC548</th>
<th>TLC549</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, $V_{CC}$</td>
<td>MIN 3</td>
<td>NOM 5</td>
<td>MAX 6</td>
</tr>
<tr>
<td>Positive reference voltage, $V_{ref+}$ (see Note 3)</td>
<td>2.5 $V_{CC}$</td>
<td>$V_{CC}+0.1$</td>
<td>V</td>
</tr>
<tr>
<td>Negative reference voltage, $V_{ref-}$ (see Note 3)</td>
<td>$-0.1$</td>
<td>0</td>
<td>2.5 $V_{CC}$</td>
</tr>
<tr>
<td>Differential reference voltage, $V_{ref+}$, $V_{ref-}$ (see Note 3)</td>
<td>1 $V_{CC}$</td>
<td>$V_{CC}+0.2$</td>
<td>V</td>
</tr>
<tr>
<td>Analog input voltage (see Note 3)</td>
<td>0</td>
<td>$V_{CC}$</td>
<td>V</td>
</tr>
<tr>
<td>High-level control input voltage, $V_{IH}$ (for $V_{CC} = 4.75$ V to 5.5 V)</td>
<td>2</td>
<td>2</td>
<td>V</td>
</tr>
<tr>
<td>Low-level control input voltage, $V_{IL}$ (for $V_{CC} = 4.75$ V to 5.5 V)</td>
<td>0.8</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>Input/output clock frequency, $f_{clock(I/O)}$ (for $V_{CC} = 4.75$ V to 5.5 V)</td>
<td>0</td>
<td>2.048</td>
<td>MHz</td>
</tr>
<tr>
<td>Input/output clock high, $t_{WH(I/O)}$ (for $V_{CC} = 4.75$ V to 5.5 V)</td>
<td>200</td>
<td>404</td>
<td>ns</td>
</tr>
<tr>
<td>Input/output clock low, $t_{WL(I/O)}$ (for $V_{CC} = 4.75$ V to 5.5 V)</td>
<td>200</td>
<td>404</td>
<td>ns</td>
</tr>
<tr>
<td>Input/output clock transition time, $t_{r(I/O)}$ (for $V_{CC} = 4.75$ V to 5.5 V) (see Note 4 and Operating Sequence)</td>
<td>100</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>Duration of CS input high state during conversion, $t_{WH}(CS)$ (for $V_{CC} = 4.75$ V to 5.5 V) (see Operating Sequence)</td>
<td>17</td>
<td>17</td>
<td>μs</td>
</tr>
<tr>
<td>Setup time, CS low before first I/O CLOCK, $t_{SU(CS)}$ (for $V_{CC} = 4.75$ V to 5.5 V) (see Note 5)</td>
<td>1.4</td>
<td>1.4</td>
<td>μs</td>
</tr>
<tr>
<td>Operating free-air temperature, $T_{A}$</td>
<td>TLC548C, TLC549C</td>
<td>0</td>
<td>70</td>
</tr>
<tr>
<td>TLC548I, TLC549I</td>
<td>−40</td>
<td>85</td>
<td>85</td>
</tr>
</tbody>
</table>

**Notes:**

3. Analog input voltages greater than that applied to REF+ convert to all ones (11111111), while input voltages less than that applied to REF− convert to all zeros (00000000). For proper operation, the positive reference voltage $V_{ref+}$, must be at least 1 V greater than the negative reference voltage, $V_{ref−}$. In addition, unadjusted errors may increase as the differential reference voltage, $V_{ref+} − V_{ref−}$, falls below 4.75 V.

4. This is the time required for the I/O CLOCK input signal to fall from $V_{IH}$ min to $V_{IL}$ max or to rise from $V_{IL}$ max to $V_{IH}$ min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 μs for remote data acquisition applications in which the sensor and the ADC are placed several feet away from the controlling microprocessor.

5. To minimize errors caused by noise at the CS input, the internal circuitry waits for two rising edges and one falling edge of internal system clock after CS↓ before responding to control input signals. This CS setup time is given by the $t_{en}$ and $t_{su(CS)}$ specifications.
electrical characteristics over recommended operating free-air temperature range,
$V_{CC} = V_{ref+} = 4.75$ V to 5.5 V, $f_{clock(I/O)} = 2.048$ MHz for TLC548 or 1.1 MHz for TLC549
(unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP†</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$ High-level output voltage</td>
<td>$V_{CC} = 4.75$ V, $I_{OH} = -360$ µA</td>
<td>2.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$ Low-level output voltage</td>
<td>$V_{CC} = 4.75$ V, $I_{OL} = 3.2$ mA</td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{OZ}$ High-impedance off-state output current</td>
<td>$V_O = V_{CC}$, CS at $V_{CC}$</td>
<td>10</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>$V_O = 0$, CS at $V_{CC}$</td>
<td></td>
<td>$-10$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IH}$ High-level input current, control inputs</td>
<td>$V_I = V_{CC}$</td>
<td>0.005</td>
<td></td>
<td>2.5</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>$V_I = 0$</td>
<td>$-0.005$</td>
<td></td>
<td>$-2.5$</td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$ Low-level input current, control inputs</td>
<td></td>
<td>0.005</td>
<td></td>
<td>2.5</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>Analog input at $V_{CC}$</td>
<td>0.4</td>
<td></td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>Analog input at 0 V</td>
<td>$-0.4$</td>
<td></td>
<td>$-1$</td>
<td></td>
</tr>
<tr>
<td>$I_{ON}$ Analog channel on-state input current during sample cycle</td>
<td>Analog input at $V_{CC}$</td>
<td>0.4</td>
<td></td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>CS at 0 V</td>
<td>1.8</td>
<td></td>
<td>2.5</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CC}$ Operating supply current</td>
<td>$V_{ref+} = V_{CC}$</td>
<td>1.9</td>
<td></td>
<td>3</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Control inputs</td>
<td>7</td>
<td>55</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$C_i$ Input capacitance</td>
<td></td>
<td>5</td>
<td>55</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

operating characteristics over recommended operating free-air temperature range,
$V_{CC} = V_{ref+} = 4.75$ V to 5.5 V, $f_{clock(I/O)} = 2.048$ MHz for TLC548 or 1.1 MHz for TLC549
(unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>TLC548</th>
<th></th>
<th>TLC549</th>
<th></th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_L$ Linearity error</td>
<td>See Note 6</td>
<td>±0.5</td>
<td>±0.5</td>
<td>±0.5</td>
<td>±0.5</td>
<td>LSB</td>
</tr>
<tr>
<td>$E_{ZS}$ Zero-scale error</td>
<td>See Note 7</td>
<td>±0.5</td>
<td>±0.5</td>
<td>±0.5</td>
<td>±0.5</td>
<td>LSB</td>
</tr>
<tr>
<td>$E_{FS}$ Full-scale error</td>
<td>See Note 7</td>
<td>±0.5</td>
<td>±0.5</td>
<td>±0.5</td>
<td>±0.5</td>
<td>LSB</td>
</tr>
<tr>
<td>Total unadjusted error</td>
<td>See Note 8</td>
<td>±0.5</td>
<td>±0.5</td>
<td>±0.5</td>
<td>±0.5</td>
<td>LSB</td>
</tr>
<tr>
<td>$t_{conv}$ Conversion time</td>
<td>See Operating Sequence</td>
<td>8</td>
<td>17</td>
<td>12</td>
<td>17</td>
<td>µs</td>
</tr>
<tr>
<td>Total access and conversion time</td>
<td>See Operating Sequence</td>
<td>12</td>
<td>22</td>
<td>19</td>
<td>25</td>
<td>µs</td>
</tr>
<tr>
<td>$t_a$ Channel acquisition time (sample cycle)</td>
<td>See Operating Sequence</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>I/O clock cycles</td>
</tr>
<tr>
<td>$t_v$ Time output data remains valid after I/O CLOCK↓</td>
<td></td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_d$ Delay time to data output valid</td>
<td>I/O CLOCK↓</td>
<td>200</td>
<td>400</td>
<td>400</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{en}$ Output enable time</td>
<td></td>
<td>1.4</td>
<td>1.4</td>
<td>1.4</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>$t_{dis}$ Output disable time</td>
<td>See Figure 1</td>
<td>150</td>
<td>150</td>
<td>150</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{bus}$ Data bus rise time</td>
<td>See Figure 1</td>
<td>300</td>
<td>300</td>
<td>300</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{bus}$ Data bus fall time</td>
<td>See Figure 1</td>
<td>300</td>
<td>300</td>
<td>300</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

† All typicals are at $V_{CC} = 5$ V, $T_A = 25^\circ$C.

NOTES:
6. Linearity error is the deviation from the best straight line through the A/D transfer characteristics.
7. Zero-scale error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
8. Total unadjusted error is the sum of linearity, zero-scale, and full-scale errors.
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT FOR 
Id, I_, AND t

LOAD CIRCUIT FOR 
I PHZ AND I PLZ

LOAD CIRCUIT FOR 
I PZL AND I PLZ

Output Under Test

Test Point

C L
(see Note A)

3 kΩ

Output Under Test

Test Point

C L
(see Note A)

3 kΩ

Output Under Test

Test Point

C L
(see Note A)

3 kΩ

VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES

VCC

50%

50%

VCC

0 V

0 V

0 V

VOLTS

I/O CLOCK

0.8 V

0.8 V

2.4 V

2.4 V

DATA OUT

Output Waveform 1
(see Note C)

50%

50%

10%

VOLTS

VCC

VOLTS

VOH

50%

50%

90%

0 V

VOLTS

VOLTS

Output Waveform 2
(see Note C)

See Note B

See Note B

See Note B

NOTES:
A. C L  = 50 pF for TLC548 and 100 pF for TLC549; C L  includes jig capacitance.
B. t en  = t PZH or t PZL , t dis  = t PHZ or t PLZ.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 1. Load Circuits and Voltage Waveforms
APPLICATIONS INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 2, the time required to charge the analog input capacitance from 0 to \( V_S \) within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

\[
V_C = V_S \left(1 - e^{-t_c/R_tC_i}\right) \tag{1}
\]

where

\[
R_t = R_s + r_i
\]

The final voltage to 1/2 LSB is given by

\[
V_C (1/2 \text{ LSB}) = V_S - \frac{V_S}{512} \tag{2}
\]

Equating equation 1 to equation 2 and solving for time \( t_c \) gives

\[
V_S - \frac{V_S}{512} = V_S \left(1 - e^{-t_c/R_tC_i}\right) \tag{3}
\]

and

\[
t_c (1/2 \text{ LSB}) = R_t \times C_i \times \ln(512) \tag{4}
\]

Therefore, with the values given the time for the analog input signal to settle is

\[
t_c (1/2 \text{ LSB}) = (R_s + 1 \text{ k\Omega}) \times 60 \text{ pF} \times \ln(512) \tag{5}
\]

This time must be less than the converter sample time shown in the timing diagrams.

![Figure 2. Equivalent Input Circuit Including the Driving Source](image_url)

\( V_I \) = Input Voltage at ANALOG IN  
\( V_S \) = External Driving Source Voltage  
\( R_s \) = Source Resistance  
\( r_i \) = Input Resistance  
\( C_i \) = Input Capacitance

\( \dagger \) Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- \( R_s \) must be real at the input frequency.
PRINCIPLES OF OPERATION

The TLC548 and TLC549 are each complete data acquisition systems on a single chip. Each contains an internal system clock, sample-and-hold function, 8-bit A/D converter, data register, and control logic circuitry. For flexibility and access speed, there are two control inputs: I/O CLOCK and chip select (CS). These control inputs and a TTL-compatible 3-state output facilitate serial communications with a microprocessor or minicomputer. A conversion can be completed in 17 µs or less, while complete input-conversion-output cycles can be repeated in 22 µs for the TLC548 and in 25 µs for the TLC549.

The internal system clock and I/O CLOCK are used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Due to this independence and the internal generation of the system clock, the control hardware and software need only be concerned with reading the previous conversion result and starting the conversion by using the I/O clock. In this manner, the internal system clock drives the “conversion crunching” circuitry so that the control hardware and software need not be concerned with this task.

When CS is high, DATA OUT is in a high-impedance condition and I/O CLOCK is disabled. This CS control function allows I/O CLOCK to share the same control logic point with its counterpart terminal when additional TLC548 and TLC549 devices are used. This also serves to minimize the required control logic terminals when using multiple TLC548 and TLC549 devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. CS is brought low. To minimize errors caused by noise at CS, the internal circuitry waits for two rising edges and then a falling edge of the internal system clock after a CS↓ before the transition is recognized. However, upon a CS rising edge, DATA OUT goes to a high-impedance state within the specified tdis even though the rest of the integrated circuitry does not recognize the transition until the specified tSU(CS) has elapsed. This technique protects the device against noise when used in a noisy environment. The most significant bit (MSB) of the previous conversion result initially appears on DATA OUT when CS goes low.

2. The falling edges of the first four I/O CLOCK cycles shift out the second, third, fourth, and fifth most significant bits of the previous conversion result. The on-chip sample-and-hold function begins sampling the analog input after the fourth high-to-low transition of I/O CLOCK. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.

3. Three more I/O CLOCK cycles are then applied to the I/O CLOCK terminal and the sixth, seventh, and eighth conversion bits are shifted out on the falling edges of these clock cycles.

4. The final (the eighth) clock cycle is applied to I/O CLOCK. The on-chip sample-and-hold function begins the hold operation upon the high-to-low transition of this clock cycle. The hold function continues for the next four internal system clock cycles, after which the holding function terminates and the conversion is performed during the next 32 system clock cycles, giving a total of 36 cycles. After the eighth I/O CLOCK cycle, CS must go high or the I/O clock must remain low for at least 36 internal system clock cycles to allow for the completion of the hold and conversion functions. CS can be kept low during periods of multiple conversion. When keeping CS low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O CLOCK line. If glitches occur on I/O CLOCK, the I/O sequence between the microprocessor/controller and the device loses synchronization. When CS is taken high, it must remain high until the end of conversion. Otherwise, a valid high-to-low transition of CS causes a reset condition, which aborts the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 internal system clock cycles occur. Such action yields the conversion result of the previous conversion and not the ongoing conversion.
PRINCIPLES OF OPERATION

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device accommodates these applications. Although the on-chip sample-and-hold function begins sampling upon the high-to-low transition of the fourth I/O CLOCK cycle, the hold function does not begin until the high-to-low transition of the eighth I/O CLOCK cycle, which should occur at the moment when the analog signal must be converted. The TLC548 and TLC549 continue sampling the analog input until the high-to-low transition of the eighth I/O CLOCK pulse. The control circuitry or software then immediately lowers I/O CLOCK and starts the holding function to hold the analog signal at the desired point in time and starts the conversion.
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